João Vieira

CPU Engineer • Ph.D. in Electrical and Computer Engineering

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Cork, Ireland

I hold a Ph.D. in Electrical and Computer Engineering from Instituto Superior Técnico, Lisbon, Portugal. Between 2015 and 2024, I have been associated with several prestigious research institutions in different countries, with my work being primarily focused on high-performance CPU, GPU, and accelerator architectures. I am currently employed by Qualcomm Ireland as a senior CPU engineer working on post-silicon PnP analysis and verification.

Previous Employment

- **Qualcomm** — Qualcomm
  Senior CPU Engineer — *Jul. 2024–ongoing*

  I am working with the CPU Post-Silicon PnP team to conduct formal performance and power analysis and verification for some of the latest Snapdragon chips. My primary focus is on Vmin/Fmax, power, and performance analysis. Specifically, my current responsibilities include:
  Vmin/Fmax: Developing and implementing automated methodologies to run various benchmarks across a range of voltage and frequency combinations to determine the minimum voltage and maximum frequency at which the Devices Under Test (DUTs) can operate and correlate with pre-silicon targets.
  Speed path determination: Identifying the root causes of voltage and frequency limitations (e.g., IR drop, timing closure issues).
  Power and Performance/Power Analysis: Measuring voltage and current drawn by the device during execution of benchmarks and correlating with pre-silicon targets. Synchronizing execution and power profiles (usually generated by different instruments) for given benchmarks, determining Regions of Interest (ROIs), and calculating performance-per-power metrics to assess the efficiency of the devices. The findings produced by this team are communicated to the Design teams, offering guidance for improvements and directly contributing to the development of future generations of Snapdragon CPUs.

- **INESC-ID** — INESC-ID
  Early-Stage Researcher — *Jul. 2015–Jul. 2024*

  I have done research on several different high-performance computing topics, namely:
  Near-Data Processing design exploration: I have developed several high-performance Processing Near Memory devices using both RTL Hardware Description Languages and FPGA prototyping and simulation resourcing to the gem5 architectural simulator and high-level hardware modeling in C++ and Python.
  FPGA-enhanced classification algorithms: I have developed a hardware accelerator targeting the kNN algorithm and prototyped it in a System on Chip, where it was integrated with a conventional CPU and memory hierarchy. The resulting system was capable of competing with commercial high-performance CPUs in terms of performance, with remarkable energy benefits.
  Control optimization of the MIPS CPU: I have implemented standard optimization techniques such as delay slots and branch prediction mechanisms on an MIPS CPU simulator written in Java.
  In total, I published seven articles in international conferences and journals while at INESC-ID.

- **University of Utah** — LNIS | UofU
  Research Assistant — *Jan. 2019–Aug. 2019*

  I have designed Functional Units to accelerate Binary Neural Networks. In particular, I have modeled such Functional Units using the gem5 architectural simulator, integrated them with an ARM Cortex A-53, and evaluated the resulting system in terms of performance and energy efficiency. This work was done in partnership with the Swiss Institute of Technology Lausanne (Switzerland) and Technion (Israel), resulting in the publication of two articles in international conferences and journals and a US patent.

- **Swiss Institute of Technology Lausanne** — LAP | EPFL
  Intern — *Feb. 2018–Sep. 2018*

  I have developed a near-cache processing system targeting low-power devices and prototyped it in an FPGA alongside a soft-CPU core, which I have also adapted for the purpose. This work was published in an international conference.

Other Relevant Experience

- **INESC-ID Data Center Support Team** — INESC-ID
  Technical Assistant — *Jul. 2022–Jul. 2024*

  My main responsibilities included hardware and software maintenance of compute servers, installation and configuration of specific software tools for research purposes, setup of new systems, and identification of required material for acquisition.

- **IST Department of Electrical and Computer Engineering Computer Labs** — SCDEEC
  System administrator — *Oct. 2015–Feb. 2018*

  I have been responsible for maintaining the IT infrastructure of a computer laboratory with over a hundred computers running both Windows and Linux systems. This experience provided me with skills in computer systems and network administration.

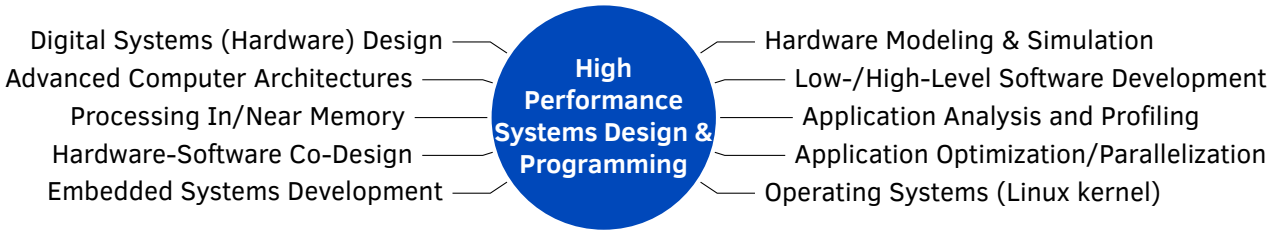
Education

- **Ph.D. in Electrical and Computer Engineering** — IST
  Instituto Superior Técnico • GPA: 18/20 • Classification: Pass with Distinction — *Feb. 2020–Apr. 2025*
- **M.Sc. in Electrical and Computer Engineering** — IST
  Instituto Superior Técnico • GPA: 18/20 — *Sep. 2013–Nov. 2018*

Training and Certifications

- **[Apr. 2025]** Emagine - Collaborating & Negotiating with Global Stakeholders
- **[Jun. 2025]** Emagine - Professional Project Management
- **[Jul. 2025]** Emagine - Communication & Presentation Skills
- **[Aug. 2025]** Semitracks, Inc. - Advanced CMOS/FinFET Fabrication
- **[Sep. 2025]** Ubuntu Linux Professional Certificate by Canonical
- **[Sep. 2025]** System Verilog for Verification
- **[Sep. 2025]** System Verilog for Design
- **[Oct. 2025]** Universal Verification Methodology
- **[Nov. 2025]** Formal Verification Essentials

Technology Skills



Example Projects

- gem5, C++, Python, Linux Kernel, Device Drivers, Computer Architectures **NDPmulator: Enabling Full-System Simulation for Near-Data Accelerators from Caches to DRAM:** IEEE Access article can be found at https://ieeexplore.ieee.org/document/10388355. Project implementation can be found in https://github.com/hpc-ulisboa/NDPmulator.
- VHDL, C, AMD Vivado, FPGA **kNN-STUFF: kNN STreaming Unit for Fpgas:** IEEE Access article can be found at https://ieeexplore.ieee.org/document/8911384. Project implementation can be found in https://github.com/joaomiguelvieira/kNN-STUFF. Awarded video can be found at https://youtu.be/SitTZdT64JI.
- C, CUDA, Python **kNNSim: k-Nearest Neighbors Simulator:** Project implementation can be found at https://github.com/joaomiguelvieira/KNNSim. An alternative Python implementation is also available at https://github.com/joaomiguelvieira/KNNSimPy.

- **VHDL**, **C**, **AMD Vivado**, **Intel Quartus**, **FPGA** **Assessing On-Chip High-Performance Interfaces on Xilinx and Intel FPGA-SoC Devices:** Project details and implementation can be found at https://github.com/joaomiguelvieira/FPGA_SoC_DMA_stress. A full report of the project can also be found at https://public.joaomiguelvieira.com/docs/reports/fpga_dma.pdf. In addition, a boilerplate for projects using Intel FPGAs–which is not provided by Intel–is provided at https://github.com/joaomiguelvieira/DE10_Standard_boilerplate.
- **Python**, **PyTorch**, **Neural Networks** **Tying Clustering and Neural Networks for more general Memory-Augmented Neural Networks:** Project full report can be found at https://public.joaomiguelvieira.com/docs/reports/mann.pdf. Due to co-authorship, the artifact of this project could not be made public.
- **C++**, **Java**, **Monte Carlo Tree Search** **Playing BlokusDuo in a ZYNQ Device: A Quest for an Efficient Algorithm:** Project implementation can be found at https://github.com/joaomiguelvieira/BlokusDuo. The article is available at https://public.joaomiguelvieira.com/playing_blokus_duo_in_a_zynq_device_a_quest_for_an_efficient_algorithm.pdf.
- **C**, **Graph Search** **ISTravel: A practical application of the Dijkstra algorithm:** Project details and implementation can be found at https://github.com/joaomiguelvieira/ISTravel.
- **Java**, **Swing** **Interactive Black Jack game:** Project details and implementation can be found at https://public.joaomiguelvieira.com/projects/videopoker/. A full report of the project can also be found at https://public.joaomiguelvieira.com/docs/reports/videopoker.pdf.
- **PHP**, **Laravel**, **JavaScript**, **HTML**, **CSS**, **SQL**, **Azure** **IST Space Management Platform:** Project details and implementation can be found at https://istspaceman.joaomiguelvieira.com/. A full report of the project can also be found at https://public.joaomiguelvieira.com/docs/reports/istspaceman.pdf.
- **C++**, **FreeRTOS**, **Electronic Design Automation**, **Arduino** **Minotaur: An Arduino-based automatic gate controller:** Project details and implementation can be found at https://github.com/joaomiguelvieira/Minotaur.
- **Network Management**, **Services**, **Linux**, **Bash** **Homelab Computer and Network Administration:** Project details and implementation available at https://web.tecnico.ulisboa.pt/~joaomiguelvieira/site/interests/.

Achievements

Publications on International Journals

- **[2024]** J. Vieira, N. Roma, G. Falcao, P. Tomas, *"NDPmulator: Enabling Full-System Simulation for Near-Data Accelerators from Caches to DRAM"*, *IEEE Access*.
- **[2023]** J. Vieira, N. Roma, G. Falcao, P. Tomas, *"gem5-accel: A Pre-RTL Simulation Toolchain for Accelerator Architecture Validation"*, *Computer Architecture Letters (CAL)*.
- **[2021]** J. Vieira, N. Roma, G. Falcao, P. Tomás, *"A Compute Cache System for Signal Processing Applications"*, *Journal of Signal Processing Systems (JSPS)*.
- **[2019]** J. Vieira, R. P. Duarte, H. Neto, *"kNN-STUFF: kNN STreaming Unit For Fpgas"*, *IEEE Access*.

Publications on International Conferences

- **[2022]** J. Vieira, N. Roma, G. Falcao, and P. Tomás, *"gem5-ndp: Near-Data Processing Architecture Simulation From Low-Level Caches to DRAM"*, *International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD 2022)*.
- **[2020]** J. Vieira, N. Roma, G. Falcao, and P. Tomás, *"Processing Convolutional Neural Networks on Cache"*, *45th International Conference on Acoustics, Speech, and Signal Processing (ICASSP 2020)*.
- **[2019]** J. Vieira, E. Giacomin, Y. Mahmood Qureshi, M. Zapater, X. Tang, S. Kvatinsky, D. Atienza, and P.-E. Gaillardon, *"A Product Engine for Energy-Efficient Execution of Binary Neural Networks Using Resistive Memories"*, *27th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC 2019)*.
- **[2018]** J. Vieira, P. Ienne, N. Roma, P. Tomás, and G. Falcao, *"Exploiting Compute Caches for Memory Bound Vector Operations"*, *International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD 2018)*.

Publications on (Portuguese) National Conferences

- **[2020]** J. Vieira, *"Playing BlokusDuo in a ZYNQ Device: A Quest for an Efficient Algorithm"*, on *XVI Jornadas sobre Sistemas Reconfiguráveis (REC 2020)*.

Book Chapters

- **[2020]** J. Vieira, E. Giacomin, Y. Mahmood Qureshi, M. Zapater, X. Tang, S. Kvatinsky, D. Atienza, and P.-E. Gaillardon, *"Accelerating Inference on Binary Neural Networks with Digital RRAM Processing"*, VLSI-SoC: EDA the New Technology Enabler, pp. 257–278, Springer, 2020.

Patents

- **[2020]** P.-E. Gaillardon, E. Giacomin, J. Vieira, "Digital RRAM-Based Convolutional Block," United States patent US11450385B2. September 20, 2022.

Languages

- **Português** *(Nativo)* ..... (10/10)
- **English** *(Proficient - TOEFL iBT 2018)* ..... (110/120)
- **Deutsch** *(Ein kleines bisschen - Goethe-Institut, Referenzniveau A2.2)* ... (4/14)

Volunteering

- **[Nov. 2021–Mar. 2023]** I was a member of AfterSchool by TreeTree2, whose purpose is to teach science to younger students and help raise the next generation of scientists and engineers.
- **[Nov. 2016, Nov. 2017]** I have participated in Web Summit (2016 and 2017 editions) as a volunteer.
- **[2013–2018]** I volunteered in three parishes. In particular, I produced advertisement material and helped with bureaucratic work.

Awards

- **[2020]** 2019 IEEE Access Best Multimedia Award
- **[2017]** 3rd place in EBEC Lisbon, category "Case Study", sponsored by McKinsey&Company

Hobbies

Electronics Repair, Re-purposing, and Recycling • 3D Design and Printing • Fossil Hunting • Hiking and Nature Exploring • Travelling

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